查询SY100E151JC供应商

FEATURES

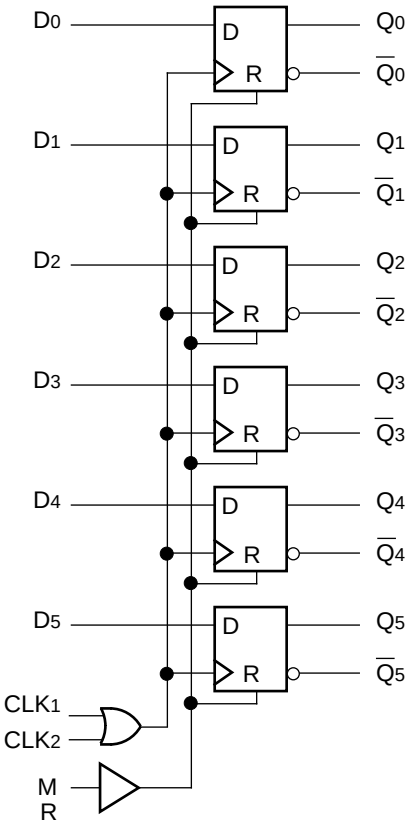
- 1100MHz toggle frequency
- Extended 100E V_{EE} range of –4.2V to –5.46V
- Differential outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E151
- Available in 28-pin PLCC package

DESCRIPTION

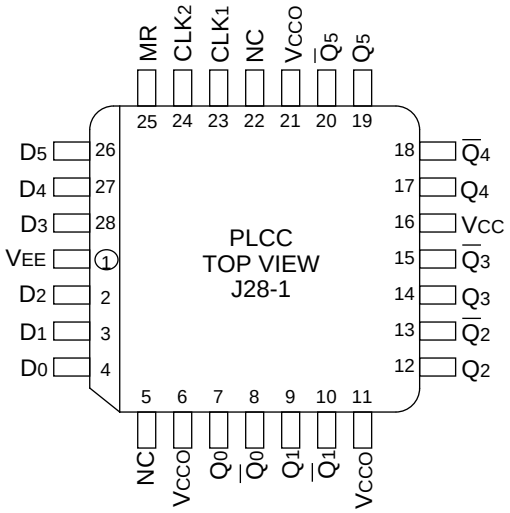
The SY10/100E151 offer 6 edge-triggered, high-speed, master-slave D-type flip-flops with differential outputs, designed for use in new, high-performance ECL systems. The two external clock signals (CLK_1, CLK_2) are gated through a logical OR operation before use as clocking control for the flip-flops. Data is clocked into the flip-flops on the rising edge of either CLK_1 or CLK_2 (or both). When both CLK_1 and CLK_2 are at a logic LOW, data enters the master and is transferred to the slave when either CLK_1 or CLK_2 (or both) go HIGH.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Outputs
V_{CCO}	V_{CC} to Output

TRUTH TABLES[1]

Asynchronous Operation

Inputs				Output
D_n	CLK_1	CLK_2	MR	$Q_n(t+1)$
X	X	X	H	L

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   t = Time before positive CLK transition
   t+1 = Time after positive CLK transition
   u = LOW-to-HIGH transition

Synchronous Operation

Inputs				Output
D_n	CLK_1	CLK_2	MR	$Q_n(t+1)$
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	$Q_n(t)$
X	u	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	65	78	—	65	78	—	65	78		
	100E	—	65	78	—	65	78	—	75	90		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	 475 475	 650 650	 800 850	 475 475	 650 650	 800 850	 475 475	 650 650	 800 850	ps	—
t_S	Set-up Time, D	0	–175	—	0	–175	—	0	–175	—	ps	—
t_H	Hold Time, D	350	175	—	350	175	—	350	175	—	ps	—
t_{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	65	—	—	65	—	—	65	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	700	300	450	700	300	450	700	ps	—

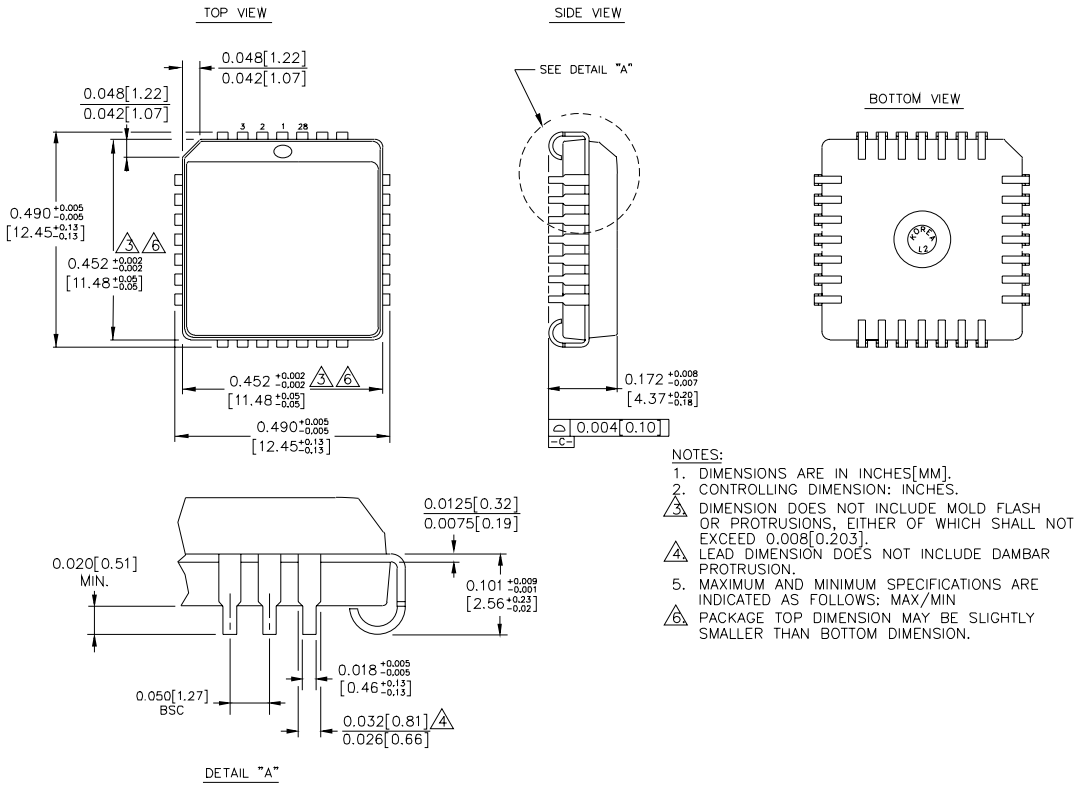
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E151JC	J28-1	Commercial
SY10E151JCTR	J28-1	Commercial
SY100E151JC	J28-1	Commercial
SY100E151JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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